

Analysis of Noise Reduction Techniques in Embedded Systems

Muhammad Aamir and Muhammad Faizan Saleem
 Sir Syed University of Engineering & Technology, Karachi.
maamir@ssuet.edu.pk and mfaizan@ssuet.edu.pk

Abstract: Finding the origin and then eliminating interfering noise in the analog domain presents a formidable challenge. Strategies for hardware and firmware noise reduction for signal conditioning paths that have sensors are discussed and developed in this paper. Moreover, noise topics such as conducted noise, device noise and radiated noise have been explored from the analog perspective.

We analyze the attributes of the offending noise in embedded systems, which are quite significant in identification of a noise source. Each category has its own set of noise reduction solutions. Graphical results are presented to demonstrate the implementation of noise reduction techniques in Embedded Systems.

This paper is a comprehensive investigation of hardware and layout techniques that provide concrete solutions to analog system noise problems.

1. Introduction

When discussing noise issues with regards to a digital circuit, topics such as transmission line reflection and ground bounce are a few of the primary topics. But generally, digital circuits operate at relatively large signal levels with high noise margins. This makes these types of circuits inherently immune to low level noise pick-up. In the analog domain, where data acquisition is performed, a small amount of external noise can cause significant interference. For instance, a difference of 10mV of noise in the analog ground between a 12-bit A/D converter and the converter's driver amplifier can cause an 8LSB error. In contrast, digital systems can tolerate hundreds of millivolts of this type of error before intermittent problems start to occur.

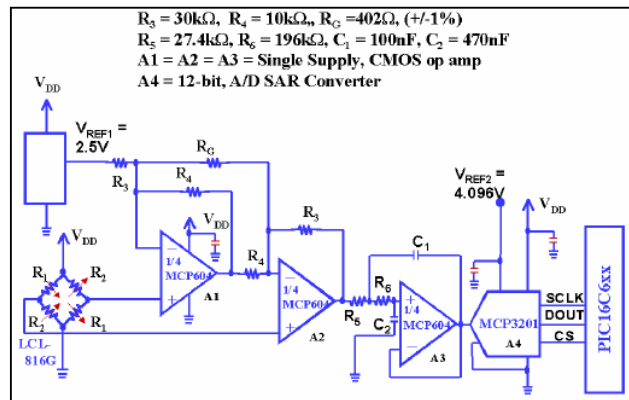
2. Data Acquisition Circuit using a Load Cell Sensor

The example circuit for this discussion is shown in Figure 1. The analog portion of this circuit consists of the load cell sensor, a dual operational amplifier (MCP602) [1] configured as an instrumentation amplifier, a 12-bit 100kHz SAR A/D converter [2] (MCP3201), and two voltage references. The A/D converter digital output is connected directly to a microcontroller SPI port.

The sensor is a 1.2k, 2mV/V load cell with a full-scale load range of ±32 ounces. In this 5V system, the electrical full-scale output range of the load cell is ±10mV. The instrumentation amplifier, consisting of two operational amplifiers (A1 and A2) and five resistors, is configured

with a gain of 153V/V. This gain, matches the full-scale output swing of the instrumentation amplifier block to the full-scale input range of the A/D converter. The SAR A/D converter has an internal input sampling mechanism. With this function, a single sample is taken for each conversion. The microcontroller [3] acquires the data from the SAR converter, performs some calibration and translates the data into a usable format for tasks such as displays or actuator feedback signals.

Figure 1: A 12-bit A/D converter can be used in



combination with an instrumentation amplifier to convert the low signal output of a sensor configured in a Wheatstone bridge to usable digital codes.

The transfer function, from sensor to the output of the A/D converter is:

$$DOUT = ((LCP - LCN)(Gain) + VREF1)(2^{12}/VREF2)$$

with $LCP = VDD (R2 / (R1 + R2))$
 with $LCN = VDD (R1 / (R1 + R2))$
 with $GAIN = (1 + R3/R4 + 2R3/R6)$

Where LCP and LCN are the positive and negative sensor outputs, $Gain$ is the gain of the instrumentation amplifier circuit. The instrumentation amplifier is configured using A1 and A2. The gain is adjusted with R_G . $VREF1$ is a 2.5V reference which level shifts the Instrumentation amplifier output $VREF2$ is the 4.096V reference, which determines the A/D converter input range and LSB size VDD is the power supply voltage and sensor excitation voltage $DOUT$ is a decimal representation of the 12-bit digital output code of the A/D converter (rounded to the nearest integer)

If the design of this system is poorly implemented, it could be an excellent candidate for noise problems. The symptom of a poor implementation is an intolerable level of uncertainty with the digital output results from the A/D converter. It is easy to assume that this type of symptom indicates that the last device in the signal chain generates the noise problem. But, in fact, the root cause of poor conversion results could originate with the other active devices or passive components, the PCB layout or even unconnected sources.

For instance, in the worst of circumstances where no noise reduction precautions are taken, the 12-bit system in Figure 1 could output large distribution of code for a DC input signal. An example of this is shown in Figure 2.

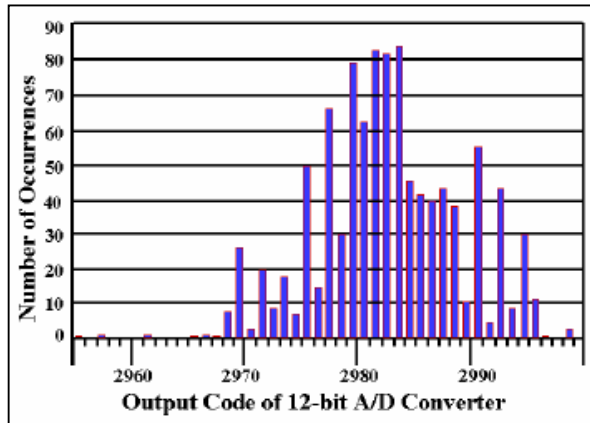


Figure 2: The poor implementation of the 12-bit data acquisition system shown in Figure 1 could easily have an output range of 44 different codes with a 1024 sample size.

The data shown in Figure:2 is far from optimum. Forty-four bits of peak-to-peak error changes the 12-bit converter system into a noise free 6.5-bit system. Averaging in the digital domain can be used to recapture the 12-bits of this system. Basically, changing a 6.5-bit system to a 12-bit system would require the averaging of $4^{(12*6.5)}$ samples or 2048 samples. If time permits, it may be possible to reduce this noise as long as the noise is Gaussian in nature.

In the analog domain, noise problems [4] can be divided into three sub-categories for discussion and troubleshooting purposes. These three categories are:

Device Noise: Noise that originates in the active or passive devices on the board.

Conducted Noise: Noise that appears on the PCB traces and needs to be addressed at that level. This type of noise originates in devices on the board or as a result of e-fields or b-fields.

Radiated Noise: Noise that is transmitted into the system via e-fields or b-fields.

3. Device Noise

Device noise can be classified into two groups, passive and active. Passive devices are constructed with materials, such as films and composites. Components such as resistors, capacitors, inductors, transformers, and conductors fall into this category. Active devices are fabricated in silicon. This class of device includes bipolar transistors, field effect transistors, CMOS [5] transistors and integrated circuits that use these transistors.

When device noise issues are described, the terminology and units of measure are somewhat different than the engineering language that is used to describe voltage, current and number of bits. The fundamental differentiation is that noise signals are by definition uncorrelated. As a consequence the simple addition of voltage or current noise sources or regions are implemented with the formula “the square root of the sum of the squares” or:

$$V_{\text{total}}^2 = V_1^2 + V_2^2 + \dots + V_N^2 \text{ or}$$

$$I_{\text{total}}^2 = I_1^2 + I_2^2 + \dots + I_N^2$$

This formula applies to noise contributions over a specific bandwidth (BW). BW is defined as the equivalent noise bandwidth. If a bandwidth is not defined, a particular frequency must be. In this case, the noise units are $V/\sqrt{\text{Hz}}$ or $A/\sqrt{\text{Hz}}$. These units of measure describe the Voltage or Current noise density (also know as spot noise). This noise is measured at a specific frequency over a 1Hz bandwidth. If the noise density across a frequency region is consistent, that noise density can be multiplied by the $\sqrt{\text{BW}}$ to convert the noise density to noise.

Peak-to-peak noise can be a calculated value or an assessment of minimums and maximums over a large sample size. A scope photo of noise over time is shown in Figure 3. Visually it can be seen that the peak-to peak noise of this sample is approximately eight divisions on the y-axis.

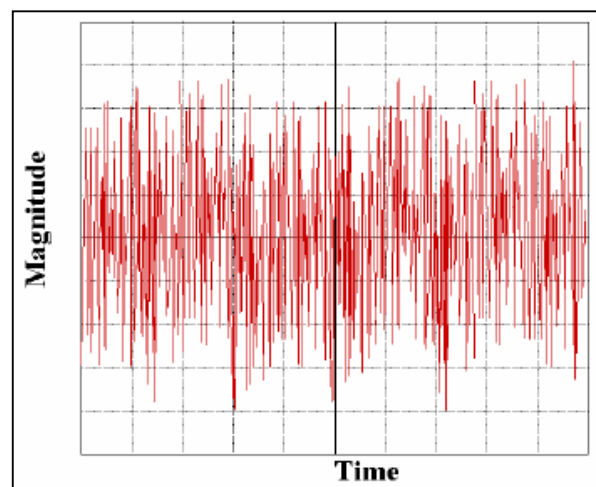


Figure 3: peak-to-peak noise value can be established by finding the maximum and minimum value of the output over a large sample size.

The peak-to-peak calculation predicts the probability that over time each occurrence of the signal in question will fall within a specified range. In the calculation, the rms value of a large sample is defined as one standard deviation of the resultant Gaussian distribution. The rms (one standard deviation) noise can then be multiplied by a constant to convert that rms number to a peak-to-peak estimate. The constant that is used is called a Crest Factor [6].

Table 1

Percent of the Time Peaks are Exceeded	Crest Factor (peak-to-peak)/(2*rms)
1	2.6
0.1	3.3
0.01	3.9
0.001	4.4
0.0001	4.9

For instance, if 4096 output samples are taken from a system that has a DC input excitation; the rms output noise is equal to one standard deviation of the 4096 samples. If this rms value is equal to $1\mu\text{V}_{\text{rms}}$, an estimate of peak-to-peak performance of the system can be calculated by multiplying the rms value times $2*\text{Crest Factor}$. A crest factor of 3.3 can be used to calculate a peak-to-peak output noise estimate of $6.6\mu\text{V}_{\text{p-p}}$ with a 0.1% probability that future samples will exceed $\pm 3.3\mu\text{V}$ centered around the average expected output. Calculated peak-to-peak noise is typically more conservative.

3.1. Passive Devices

Resistors: There are three basic classes of fixed resistors: wire wound, film type and composition. Regardless of their construction, all resistors generate a noise voltage. This noise is primarily a result of thermal noise. The lower quality resistors, such as the composition type, have additional noise in the lower frequency spectrum due to shot and contact noise. Thermal noise, which is also called Johnson noise, is generated by the random thermal motion of electrons in the resistive material and can never be lower than ideal. It is independent of dc current flow and is constant across the entire frequency spectrum.

The ideal thermal or Johnson noise for resistors is:

$$V_N = \sqrt{4KTR(BW)}$$

Where K is equal to Boltzman's constant, which is $1.38e^{-19}$

T is equal to temperature in Kelvin

R is the resistance value in ohms

(BW) is the noise bandwidth of interest

The ideal calculated noise of various values of resistance is shown in Table 2.

Table 2: Ideal Resistance Noise @ 25 ° C (298.16 ° Kelvin)

Resistance (Ω)	Noise Density (nV/√Hz)	Resistance (Ω)	Noise Density (nV/√Hz)
1	0.1283	100	1.283
2	0.1814	200	1.814
3	0.2222	300	2.222
4	0.2566	400	2.566
5	0.2869	500	2.869
6	0.3142	600	3.142
7	0.3394	700	3.394
8	0.3629	800	3.629
9	0.3849	900	3.849
10	0.4069	1000	4.069
20	0.5737	2000	5.737
30	0.7027	3000	7.027
40	0.8114	4000	8.114
50	0.9072	5000	9.072
60	0.9937	6000	9.937
70	1.0734	7000	10.73
80	1.1475	8000	11.48
90	1.4813	9000	14.81
100	1.2829	10000	12.83

Wire wound resistors are the quietest of the three and come close to ideal noise levels. Composition resistors are the noisiest because of their contact noise, which is aggravated by current. Otherwise composition resistors have the same noise as wire wound.

Spice simulations can be used to perform “what ifs” with device noise problems such as resistor noise. The total noise contribution of the instrumentation amplifier structure in Figure 1 from DC to 10MHz is $814\mu\text{V}_{\text{rms}}$ and $677\mu\text{V}_{\text{rms}}$ from DC to 100kHz. If the resistors in this circuit are increased by 10X the total noise contribution of this circuit is $930\mu\text{V}_{\text{rms}}$ out to 10MHz and $728\mu\text{V}_{\text{rms}}$ out to 100kHz. If the resistors are reduced by 10x, the total noise contribution is $787\mu\text{V}_{\text{rms}}$ to 10MHz and $671\mu\text{V}_{\text{rms}}$ out to 100kHz. If a low pass anti-aliasing filter is not used in this circuit, the noise contribution due to the resistors in Figure 1 is significant.

Capacitors: In noise discussions, capacitors are generally identified as the device that reduces or filters system noise. Capacitors are most frequently categorized by the dielectric material that they are made of. Each type of capacitors has characteristics that make them suitable of certain applications.

For instance, the large capacitance values of electrolytic capacitors in a small case offer a distinct advantage in terms of board layout. They are most often used for low frequency filtering, bypassing and coupling. As a disadvantage, electrolytic capacitors are polarized and a DC voltage must be maintained across them. In contrast, the series resistance of paper and Mylar capacitors is considerably less than electrolytic capacitors. These capacitors are medium frequency devices and useful up to a few megahertz. Paper and Mylar capacitors are typically used for filtering, bypassing, coupling, timing and noise suppression. Mica and ceramic capacitors have very low series resistance and inductance. These are high frequency devices that are useful up to about 500MHz if the leads are kept short. These capacitors are usually used for high-frequency filtering, bypassing, coupling, timing and frequency discrimination. They are also very stable with respect to time, temperature and voltage. Polystyrene capacitors have extremely low series resistance and very stable capacitance-frequency characteristics. These devices are the closest to the ideal capacitor. Typical applications include filtering, bypassing, couple, timing and noise suppression.

Inductors and Transformers: An ideal inductor would only have inductance, but actual inductors also have series resistance and distributed parallel capacitance between windings. An important characteristic is their susceptibility to and generation of stray magnetic fields. Two inductors that are intentionally coupled form a transformer. Transformers are usually used to provide isolation between two circuits, by breaking ground loops or signal paths or power generation. These devices are typically noise generators because of the switching activity associated with isolation.

3.2. Active Devices

Pure Analog Devices – This category of devices include operational amplifiers, instrumentation amplifiers, voltage references, voltage regulators, to name a few. These devices are typically specified in terms of nV/\sqrt{Hz} , pA/\sqrt{Hz} , μV_{rms} or μV_{p-p} . The noise that is generated by these devices can be defined as current noise or voltage noise, both of which have two fundamental regions. The two fundamental regions of noise that these devices produce are the $1/f$ and broadband regions.

$1/f$ noise is also known as contact noise or flicker noise. This is low frequency noise where the power density varies as the reciprocal of frequency ($1/f$). This noise is a consequence of trapped carriers in the semiconductor material, which are captured and released in a random manner. The time constant of this energy is concentrated within lower frequencies. $1/f$ noise is shown graphically in Figure 4.

Shot noise on the other hand is associated with the DC current flow across a p-n junction. This noise is due to

random diffusion of carriers through the base of the transistor and random generation and recombination of hole electron pairs. The rms noise current is equal to $ISH = \sqrt{2qIDC (BW)}$, where q is electron charge ($1.6e-19$

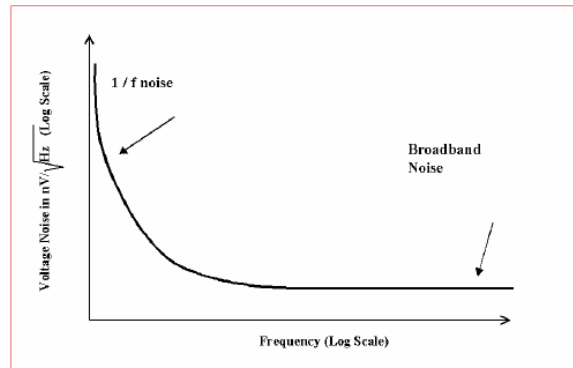


Figure 4: Noise contributions from devices across the frequency spectrum emulated a $1/f$ characteristic at low frequencies and a flat response at the higher frequencies.

coulombs), IDC is the average DC current in amperes, and (BW) is the noise bandwidth in Hertz. The noise contribution from this source is generally seen in the higher frequencies or the broadband area shown in Figure4.

4. Conducted Noise

Conducted noise is the noise that is present on the PCB traces. Many times conducted noise problems can be corrected at the point of origin, whether it is replacing a noisy device or changing the environment in order to eliminate an emission problem. However, there are circumstances where this is impossible because of the primary purpose of a particular device or the nature of the environment. For instance, an electrically isolated system needs isolated power that spans from one side of the barrier to the other. This type of isolation is provided with a DC/DC converter. A by-product of every DC/DC converter is switching noise on the power supply. Elimination of the DC/DC converter will remove the noise from the circuit but it will also remove the isolation barrier. Lower noise DC/DC converters are available on the market, however, the switching noise from this type of device is a standard by-product. Given this type of problem, there are techniques that can be used to minimize noise interference once it is present on the PCB traces.

4.1. Power Supply Filter Strategies

Regardless of the power supply source, good circuit design implies that by-pass capacitors are used. This is true in all cases. For instance, a regulator, DC/DC converter, linear or switching power supply can provide the power to the board. In all of these cases, by-pass capacitors are a required part of the design. If they are not included, the power supply noise may very well eliminate any chance for reliable circuit performance.

By-pass capacitors belong in two locations on the PC board; one at the power supply (10 μ F to 100 μ F or both) and one for every active device (digital and analog). The value of the device's by-pass capacitor is dependent on the device in question. Generally speaking, if the bandwidth of the device is less than or equal to \sim 10MHz, a 0.1 μ F by-pass capacitor will reduce injected noise dramatically. If the bandwidth of the device is above \sim 50MHz, a 0.01 μ F by-pass capacitor is probably appropriate. In between these two frequencies, both or either one could be used. In all cases, it is best to refer the manufacturer's guidelines for specifics.

The leads of the device's by-pass capacitor must be placed as close as possible to the power supply pin of the device. If two by-pass capacitors are used for one device, the smaller of the two should be closest to the device pin. Finally, the lead length of the by-pass capacitor should be as short as possible in order to minimize lead inductance.

4.2. Signal Path Filtering Strategies

A system such as the one shown in Figure 1 must have an analog filter, however, it can also have a digital filter that can be used to improve the accuracy of the system. The analog filter is always implemented in the signal path prior to the analog-to-digital converter. In contrast, if a digital filter is implemented, it is done after the conversion from analog-to-digital has occurred. There are a number of system differences that the designer should be aware of when the filtering function is provided in the digital domain rather than the analog domain.

The primary function of the low pass analog filter in Figure 1 is to remove the high frequency components of the input signal to the A/D converter. If these high frequencies pass to the A/D converter, they will contaminate the conversion data by aliasing during the conversion process. To illustrate this, a two pole anti-aliasing filter is added (per the circuit in Figure 1) to the board that was used to illustrate the poor circuit implementation (Figure 2). This board is still missing its ground plane and by-pass capacitors; however, the noise level in data conversion process has improved dramatically as is shown in Figure 5.

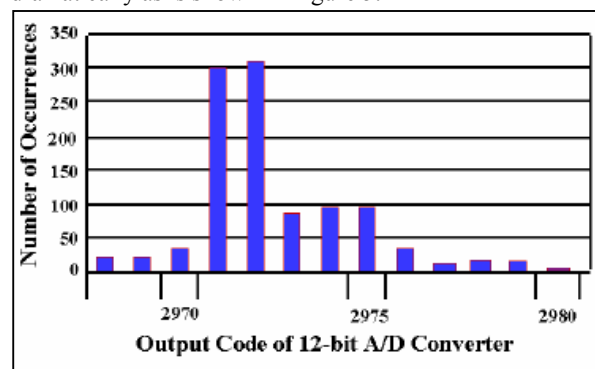


Figure 5: Once a second order, low-pass filter is included in the circuit, the data acquisition system in Figure 1

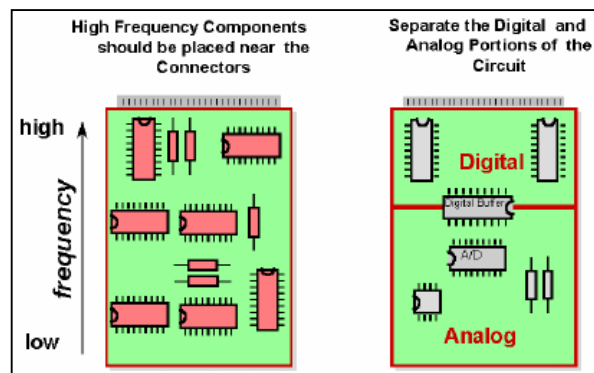
changes from a 6.5-bit system to an 8.3-bit system. This layout implementation of the circuit lacks the ground plane and by-pass capacitors.

Analog filtering can also remove noise that is superimposed on the analog signal before it reaches the A/D converter. In particular, this includes extraneous noise peaks. This reduces the possibility of input signal noise saturating the analog modulator of the A/D Converter.

Once again, a simple averaging digital filter can reduce this noise. In the case above (Figure 5), 12-bits can be achieved by averaging $4^{(12 - 8.3)}$ samples or 169 samples. Since digital filtering occurs after the A/D conversion process, it can also remove noise that has been introduced into the conversion process. A digital filter uses over sampling and averaging techniques to reduce in band and out of band noise. Also, the digital filter can be made programmable far more readily than an analog filter. Depending on the digital filter design, this gives the user the capability of programming the cutoff frequency and output data rates.

4.3. Layout Strategies

Device placement is critical. In general, the circuit devices should be separated into two categories: high speed (>40MHz) and low speed. Once this separation is done, the devices should once again be separated into three sub-categories: pure digital, pure analog, and mixed signal. The board layout strategy should map the diagram shown in Figure 6. Notice the relationship of digital versus analog and high speed versus slower speeds to the board



connector.

Figure 6: If precision is critical, care should be taken when placing the active devices on a PCB. High speed and digital devices should be placed as close to the connector as possible.

The digital and analog circuitry should be separated as it is shown Figure 6. The pure analog devices are furthest away for the digital devices and the connector to insure that digital switching noise is not coupled into the analog signal path through the traces or ground plane.

A/D converter layout techniques vary from with converter technology. When SAR A/D Converters are used, the entire device should reside on the analog power and ground planes. A/D converter vendors many times will supply analog and digital ground pins. These pins are designed to move interfering currents off of the chip and are not intended to be connected between the PCB analog and ground planes. If high resolution SAR converters are used, a digital buffer should be used to isolate the converter from bus activity on the digital side of the circuit.

In contrast, if the A/D Converter is designed using a delta-sigma technology, it should straddle the analog and digital planes. This is due to the fact that the Delta-Sigma Converter is primarily a digital IC.

5. Emitted or Radiated Noise

Noise can enter the circuit through a second method, radiation. The level of susceptibility of the circuit to extraneous noise is directly related to the implementation of signal traces across the board, ground plane and power plane strategy, and subtleties such as the use of differential signal paths and shielding.

5.1. Signal Traces

As a basic guideline, both analog and digital signal traces on PC boards should be as short as possible. Shorter traces minimize the susceptibility of the circuit to on-board and extraneous signals. The amount of extraneous noise that can influence the PCB is dependent on the environment. Opportunities for on-board signal coupling, however, can be avoided with careful design. One set of terminals to be particularly cautious of are the input terminals of amplifiers and A/D converters. The problem arises because these terminals typically have high impedance inputs. As an example, the input terminals (IN+ and IN-) of an operational amplifier are extremely sensitive to coupled noise. The magnitude of the input resistance of these terminals is typically 10^9 to $10^{13} \Omega$.

Signal coupling problems occur when a trace that has a high impedance termination is next to a trace that has fast changing voltages, such as a digital or clock signal. In this situation, charge is capacitively coupled between the traces per the formula:

$$I = C\delta V/\delta t$$

Where I is current in amperes; C is capacitance
 δV is change in voltage; δt is change in time

Figure: 7 illustrates how the value of the capacitance between two traces can be calculated. This capacitance is primarily dependent on the distance (d) between the traces and the distance that the two traces are in parallel (L).

5.2. Ground and Power Supply Strategy

The definition and implementation of a ground plane and power supply strategy of a board layout is critical when designing low noise solutions [7]. This is illustrated with the data presented in Figure 2 and Figure 5. Both sets of

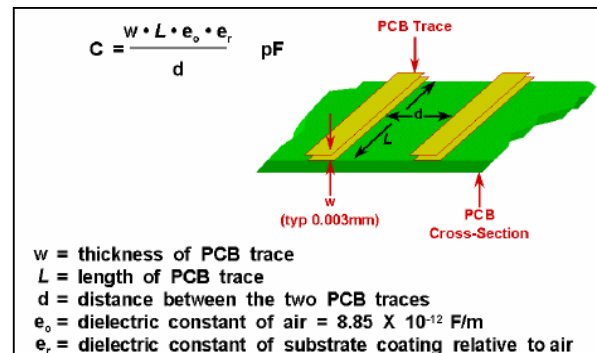


Figure 7: Every time two traces are placed in close proximity on a PCB, a capacitor is constructed. If one of the two traces is high impedance, interfering noise will be coupled into the circuit.

data were taken with a board that did not have a ground plane. Assuming that a ground plane is not needed is a dangerous assumption in any circuit with analog and/or mixed signal devices. Ground planes solve problems such as offset errors, gain errors, and noise problems. These errors are more prevalent than with a lack of a power supply plane, because analog signals are most typically referenced to ground. For instance, this author's ground plane-less implementation of the circuit shown in Figure 1 has difference of 3.70mV across the 4" x 4" board. This is equivalent to 3.7 bits of offset error by the time the signal gets to the 12-bit A/D converter (MCP3201).

When determining the grounding strategy of a board, the task at hand should actually be to determine if the circuit can work adequately with just one ground plane or does it need multiple planes. If the circuit has a "minimum" amount of digital circuitry on board, a single ground plane and a single power plane may be appropriate. The board designer defines the qualifier "minimum". The danger of connecting the digital and analog ground planes together is that the analog circuitry can pick-up the noise from the return currents, which can couple into the analog signal path. In either case, the analog and digital grounds and power supplies should be connected together at one or more points in the circuit.

The inclusion of a power plane in a 12-bit system is not as critical as the required ground plane. Although a power plane can solve many problems, power noise can be reduced by making the power traces two or three times wider than minimum trace widths on the board and by using by-pass capacitors effectively.

In Figure 8, the circuit from Figure:1 has been implemented on a board with the ground plane, low pass filter, and by-pass capacitors included. Signal traces from

the board in Figure 1 to the board in Figure 8 have not been changed.

6. Conclusion

In summary, circuit noise problems can originate from a variety of sources. With careful examination of the

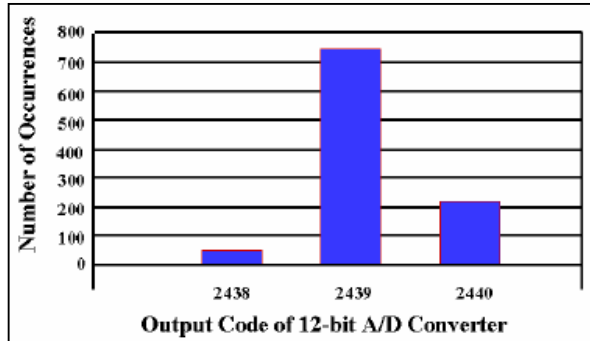


Figure 8. When noise reduction techniques are used when implementing the circuit in Figure 1, it is possible to get at least a 10.4-bit system.

attributes of the offending noise, the source can be identified and noise reduction solutions become more apparent. There are three subcategories that noise problems can be divided into. These categories are Device noise, Conducted noise and radiated noise. Each category has its own set of noise reduction solutions.

If an active or passive device is identified as the major noise contributor, lower noise devices can be substituted into the circuit. If device replacement is not feasible, the noise becomes conducted noise. Conducted noise is

present in the PCB trace. This type of noise can be reduced using techniques such as by-pass capacitors, analog filters, digital filters, or rearranging the position of the devices on the board with respect to the power connectors and signal path. Radiated noise is injected into the circuit via e-fields or b-fields. The contribution of this type of noise can be minimized with a careful layout that avoids signal-coupling opportunities, inclusion of ground and power planes and system shielding techniques.

7. References

- [1] Microchip Control Handbook, Microchip Technology Incorporated, 2004.
- [2] 12 Bit A/D Converter with serial interface, Data Book, Microchip Technology Incorporated, 2001.
- [3] Martin Bates, PIC Micro controllers, Second Edition, Book News, Inc, 2004.
- [4] Morrison, Ralph, Noise and Other Interfering Signals, John Wiley & Sons, Inc., 1992.
- [5] Allen, Holberg, CMOS Analog Circuit Design, Holt, Rinehart and Winston, 1987
- [6] John G. Webster, Electrical Measurement Signal Processing, & Displays, 2003.
- [7] Stuart Ball, Analog Interfacing to Embedded Microprocessors: Real World Design, Newnes, 2001.