Integration of Passives for Receiver Front-End for 5GHz Wireless LAN Applications

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Abstract: *The transceivers for future technology (third generation cellular, wireless LAN) need to be portable (compact), battery-powered and wireless. The present single-chip solutions for RF front-ends do not yield complete system integration.*

A system-on-a-package (SoP) approach can solve these problems. High quality components can be integrated in the package. This paper reports a fully integrated single-package RF prototype module for a 5 GHz WLAN receiver front-end, which is intended to demonstrate the concept of SoP integration. The approach that is illustrated here is implemented with a thin film multichip module (MCM-D) interconnect technology. This technology also allows the integration of high quality passive components. With these passives, low-loss filters can be implemented.

Keywords: *Low noise amplifier, bandpass filter, chip-package co-design, downconverter, MCM-D, RF front-end, system-on-chip, system-on-package, transceiver.*

I INTRODUCTION

Wireless communication requires better performance, lower cost, and smaller RF front-end size. Although much effort has been devoted to realization of SoC (System-on-Chip) in RF areas using Si based technology, SoC is considered a solution for limited applications, such as Bluetooth. The recent development of materials and processes in packaging makes it possible to bring the concept of System-on-Package (SoP) into the world to meet the stringent needs of wireless communication. RF-SoP provides a complete packaging solution for RF module by integrating embedded passives components and MMIC at the package level. Using SoP approach we can achieve low cost by using embedded passive instead of discrete components, design flexibility for MMIC by using high-Q passives embedded in the package, minimized loss and parasitic effects by reducing the number of interconnections, reduced module size by adopting multilayer packaging, ease of realization of multifunctional RF modules in a single package better high-power handling capability than MMIC chip.

RF-SoP is "to provide a complete packaging solution for RF module by integrating embedded passives components and MMIC at the package level" [1], [2]. The recent development of materials and processes in packaging makes it possible to bring the concept of SoP into the RF world to meet the stringent needs of wireless communication [3].

The System-on-Package approach has emerged as the most effective to provide a realistic integration solution because it is based on multilayer technology using low-cost and high-performance materials [3]-[5]. Multilayer topology high-density hybrid interconnect schemes, as well as various compact passive structures, including inductors, capacitors, and filters, can be directly integrated into the substrate. Thus, a high-performance module can be implemented while simultaneously achieving cost and size reduction [3].

The challenge in SoC is not how many transistors can be built on a single chip, but rather how to integrate diverse technologies together, predictably and cost effectively. It is clear that integrating all sub-blocks with different technologies on a single die (SoC) may not be the best choice, especially in RF/wireless applications (such as integrating RF front-end with digital blocks). The generalization of SoC---SoP and its design methodology—Chip-package co-design could solve such problems of SoC. They are one of the most important research trends in today's RF/wireless technology.

The approach implemented here exploits the concept of Chip package co-design [6], [7]. This approach uses high-quality passive components that are realized in a thin-film MCM (MCM-D) interconnection technology. Passive components such as individual inductors and also complete RF bandpass filters are directly integrated into the MCM substrate (Glass substrate is used having εr = 4.6). The quality factors 'Q' of the passive components are very high, especially compared to on-chip passive components. The MCM technology features high quality inductances between 1 and 40 nH. Compared to a standard thick-film technology or a low-temperature cofired ceramic (LTCC) technology, this high-resolution thin-film MCM-D technology features smaller component tolerances, also at GHz frequencies. At the same time, the MCM substrate is a carrier for the integrated circuits that are mounted on this substrate preferably with a flip-chip technique. The high quality factor of passive components that are realized in the MCM-D technology enables a successful integration of RF filters with an acceptable insertion loss in the passband, which is not the case with a SoC approach. The integration of a front-end on an MCM-D module that uses high-quality passive components enables the use of the proven-good superheterodyne architecture. The front-end comprises two bandpass filters, a low noise amplifier (LNA) and a downconversion mixer, as shown in Figure. 1. The active components are commercially available, “bare die” components [8], [9], which are flip-chip mounted onto the MCM substrate.

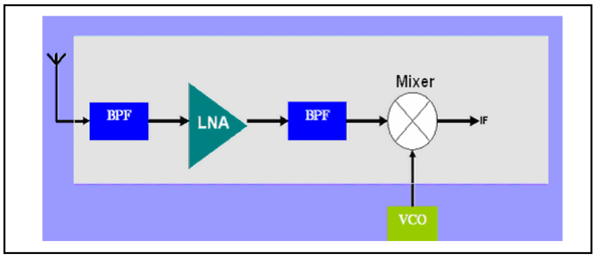

Figure 1: Block diagram of the receiver front-end for 5 GHz

The MCM module integrates some passives for the active circuits, impedance matching for the LNA and two lumped-element bandpass filters. The two integrated bandpass filters avoid the use of discrete RF filters, which are still required in “single-chip” solutions. This minimizes the number of components to be mounted. The 5.25 GHz RF input signal is downconverted to a fixed intermediate frequency (IF) of 500 MHz. The IF frequency is kept fixed by ranging the local oscillator (LO) frequency depending on which channel is to be received. The measurements are done for an LO frequency around 4.75 GHz. This means that the so called image frequency for the mixer lies around 4.25 GHz, which is the difference of the (variable) LO frequency and the (fixed) IF frequency. Since the downconverter is as sensitive to the RF frequency as to the image frequency, the signal components at the image frequency must be rejected. This is accomplished with one or more bandpass filters, centered on the RF frequency. The largest problem of single-chip integration lies in the integration of the passives for high frequencies. Partitioning a system over a number of chips, which can still be mounted in a single package, also circumvents substrate coupling since the conductive silicon substrate is replaced by a glass substrate that is almost a perfect insulator. In addition, one does not have to stick to one IC-technology. Every component is integrated in the best-fitted technology.

Chip-package co-design optimizes the integration of circuits and systems more effectively than traditional design methods. It is an important concept from the system perspective since the final module’s performance should be optimized, not just the chip or the package. Co-design has several advantages to high frequency circuit design: optimized performance, better design accuracy, and a reduced number of design iterations [7].

II AN MCM-D SUBSTRATE AS A CARRIER

Deposited thin-film multilayer. An MCM-D substrate technology has been employed in this work. The MCM-D technology developed by GEC Plessey Semiconductors has been described in detail elsewhere [10]. One of the constraints on the design of integrated RF systems is the availability of suitable and cost effective components. The system builder is also facing demand for ever greater functional density in RF products, particularly for portable products such as mobile phones and sub notebook computers [11]. MCM-D technology offers many of the necessary components and also gives advantages of size, repeatability and externally component count reduction. The MCM-D technology [Figure 2] allows the integration of different families of ICs together with integrated passive components to produce miniature radio modules and RF functions which offer considerable size and performance advantages over conventional discrete solutions [12], [13]. The benefits are further enhanced by the use of MCM-D passive components to produce structures such as filters which would normally consume significant space and cost in a conventional design [12]. MCM-D processes have been offering 4 to 10 fold reductions in the area of RF functions when compared to the surface mounted equivalent [14]. MCM-D technology as a solution for use in RF systems offers many significant advantages over more traditional technologies. In particular the size reductions and performance improvements possible allow product developers to meet more closely the requirements of the marketplace. The Technology then eases many of the design problems in bringing RF systems into production [12].

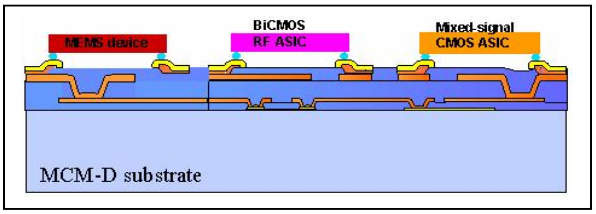

Figure 2. MCM-D Technology.

III SPECIFICATIONS OF A 5GHZ WLAN

Standardization activities for wireless local area networks (WLAN) in the 5 GHz ISM band have been evolving for a few years already. The American IEEE and European ETSI organizations are finalizing their respective standards for the 5 GHz band: IEEE 802.11a [15] and HIPERLAN/2 [16]. These two standards define nearly identical systems, based on orthogonal frequency division multiplexing (OFDM) modulation. OFDM is a multicarrier modulation technique that efficiently manages intersymbol interference and multipath distortions, making it very suited for indoor wireless communications. The standards foresee several data rates up to 54 Mbps, using different modulation schemes at different coding rates. The modulation schemes can be binary phase shift keying (BPSK), quadrature phase shift keying (QPSK) and quadrature amplitude modulation with 16 (16-QAM) and 64 points (64-QAM). The IEEE 802.11a standard defines three frequency bands that can be used. A first band extends from 5.15 to 5.25GHz, the second from 5.25 to 5.35 GHz and the third from 5.725 to 5.825 GHz. HIPERLAN/2 specifies two bands: from 5.15 to 5.35 GHz and from 5.470 to 5.725GHz. Our design only considers the frequency range from 5.15 to 5.35 GHz, which is common to both standards. This band is divided into eight channels with a nominal spacing of 20 MHz. The IEEE 802.11a standard specifies further that the receiver should be able to receive a signal between -85 dBm and -30 dBm at the antenna and that the noise figure of the whole analog receiver chain should be less than 10 dB. Apart from that, the receiver must be able to withstand the effects of out-of-band blocking signals up to 0 dBm [17].

The design tool is Agilent ADS (advanced design system). ADS is a powerful and one of the most popular CAD tools in industry for wireless system design. The starting point for the presented SoP approach is a multichip module (MCM) technology. A substrate with low losses is required for RF applications. Here, a thin-film technology (MCM-D) with an Orosilicate glass substrate is used. This is a low-cost material with high resistivity and low microwave loss. The lithographic nature of a thin film technology guarantees lower component tolerances [18] in comparison with standard thick film or low temperature co-fired ceramic (LTCC) processes. The design has been realized using SiO2 as dielectric materials (εr = 3.9).

The package substrate provides a good environment for integrated passive elements. Resistors, capacitors, and inductors can be fabricated on the substrate with a thick-film or thin-film process. In principle, all passive subcircuits can be built on package substrates with connections to on-chip active subcircuits. The partition of what functions are on or off chip should be determined by the optimization of cost, size, and performance. Usually, the passive components and subcircuits on package substrates have higher quality factors than their on chip counterparts. However, full integration on a chip usually means lower cost and smaller size [7].

IV DESIGN OF PASSIVE COMPONENTS

Integration of passive elements in a package is the most important factor in chip-package co-design's success. Without this technology, chip and package designs are nearly independent. With the ability to integrate resistors, inductors, capacitors, and distributed transmission-line elements, chip and package designs couple closely. Chip designers can then move critical passive elements that require high quality factors and large space off the chip. This improves circuit performance and potentially saves costs [7].

The conventional planar spiral inductor has been fabricated on a single layer. Increasing inductance has been obtained by increasing the number of turns laterally. As the area increases proportionally to the number of turns, Rs, Cs, and Ls increase while Rp decreases. Therefore, this topology is expected to have both low Q and self-resonance frequency (SRF). One of the important factors of an inductor is the quality factor (Q). High Qs at the frequency range of interest can be obtained by designing multilayer inductors [3]. In this design both multilayer as well as single layer inductors has been designed. Therefore, results for extremely compact 0.5(Single Layer) and 1.5-turn(Multilayer) inductors having a line width of 90 µm and 40 µm respectively. For 0.5-turn inductor, the Q is 64 and the inductance, Leff, is 1.4 nH at 5.25 GHz and for 1.5-turn inductor, the Q is 31 and the inductance, Leff, is 3.0 nH at 5.25 GHz. Also, the thick Aluminum metallization in the packaging process made it possible to get a very high-Q. This has decreased the shunt parasitic capacitance and reduced the eddy current flowing in the ground plane, producing negative mutual inductance effect. As a result, higher Q and Leff have been achieved [2]. The inductors used for filter design have been designed on single layer because the metal layer 1 is only 0.5 µm thick whereas, the inductors used for Low noise amplifier have made use of both layers because high inductances as well as better Q were required at the same time.

The inductors have been made in the metal 2 layer (3 µm thick Aluminum). The inductor values range between 0.3 to 3.6 nH, with a maximum quality factor Q up to 64 at 5.25 GHz. The frequency of maximum Q and the maximum value of Q itself can be exchanged. Inductors with lower values have higher Q values, because they can be smaller (lower parasitic) or use wider metal tracks. An inductor with a larger inductance value using wider tracks would suffer a lower frequency of self-resonance due to higher parasitic capacitance. Therefore, inductors with lower inductance values can have higher Q-factors, given a certain technology and application (i.e., the required operation frequency).

V BANDPASS FILTER DESIGN

Filters are essential components in many electrical circuits. For RF and low microwave applications, the filters may be realized by combinations of capacitive and inductive lumped passive components [19]. These passive filters may then be integrated in the MCM-D interconnection substrate, creating a functional interconnection. We have designed Embedded MCM, lumped element filters. Since we are looking at the two lower frequency bands only, the passband of interest ranges from 5.15 to 5.35 GHz. Implementing this design in a planar technology such as MCM-D imposes some restrictions. For any device in front of the low noise amplifier (LNA), the insertion loss should be minimized, since the value of the insertion loss (expressed in dB) directly adds to the noise figure of the complete receiver with same amount. A sixth-order filter in MCM-D would have too much insertion loss, due to losses in the passives. Therefore, the RF bandpass filter for the receiver is split into two filters, one second-order filter in front of the low noise amplifier (LNA) and a second one after the LNA. A second-order bandpass filter with lumped elements is realized. The design actually consists of two parallel LC resonators, which are coupled to each other and to their input and output terminals with capacitors. The inductors must have a high quality factor for the filter to have low loss. The quality factor drops with increasing inductance. On the other hand, the inductor cannot be too small. The LC tank determines the center frequency, which needs to be kept constant (at 5.25 GHz). A smaller inductor implies a smaller capacitor, which in turn is related to the required coupling capacitance. To have a good reproducibility and robustness against process tolerances, this coupling capacitance may not become too low. The values of the LC-tank components are respectively 1.38nH and 485fF. The capacitor that couples the two resonators has a value of 46fF and the input and output coupling capacitances equal 156fF. In order to select the appropriate bandwidth and center frequency of passband, analysis has been done by considering different design implementations. The inductors used have wide conducting path so that they must offer less resistance and by doing so, Q of the inductors has increased. Moreover, to increase the Q to achieve the required value, inductors have been made wider [7] although this approach leads to the inductors which occupy more area, but by using smaller area the Q of the inductor was not high enough to meet the design requirements. More precisely, low Q value of inductors lead to higher insertion loss of the filter. The Q of the capacitors is not of much concern in this design, as it has been high enough that the designed capacitors have gave almost values closer to their ideal models. The layout design of the filter is shown in Figure 4.

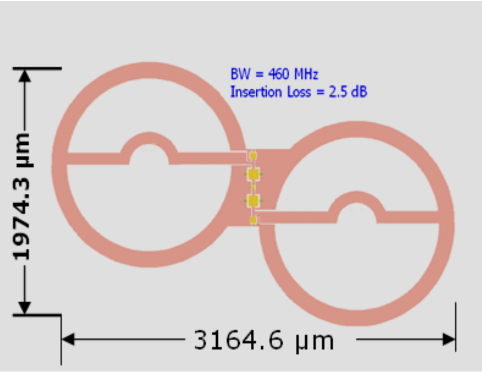

Figure 4. Bandpass filter layout design

The measurements [Figure 5] of this filter show an insertion loss of -2.5 dB and bandwidth of 460 MHz. The return loss in this frequency band is better than 13 dB.

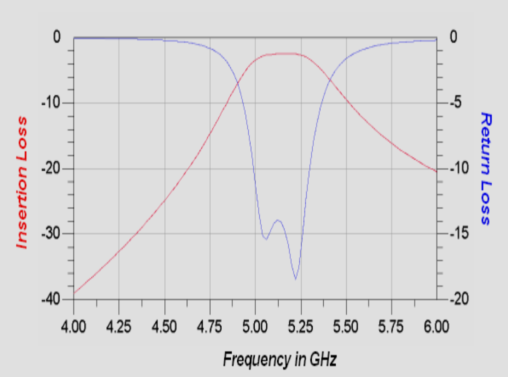

Figure 5. Insertion loss & return loss

By comparing this filter with [17], it has good result even though in this design aluminum metal is used than copper in [17]. There has been acceptable compromise on bandwidth and insertion loss because in order to further improve the design the size of the filter has been increasing beyond the acceptable values

VI LOW NOISE AMPLIFIER DESIGN

Amplifier designs at RF differ significantly from the conventional low-frequency circuit approaches and consequently require special considerations. The stabilization has been achieved by using a series resistor at the output port. The data available from the manufacturer of amplifier [8] was scattering parameters values at different frequencies and not much information that we could use transistor model. The low noise amplifier is built around a GaAs PHEMT [8]. After determining the required input and output impedances the next step is to achieve that impedance with a certain combination of passive elements. The layout of LNA is shown in Figure 8. and the measurement data is shown in Figure 9.

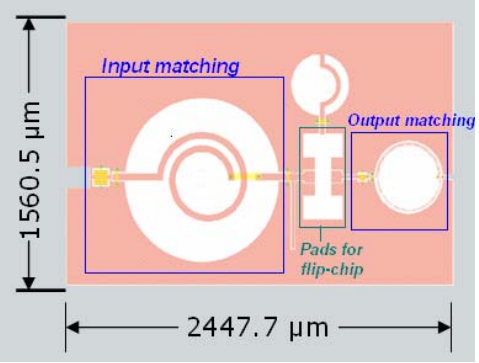

Figure 8. LNA layout using

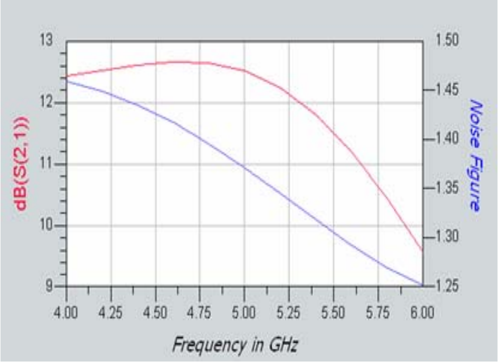

Figure 9. LNA Gain and Noise Figure.

VII RECEIVER FRONT-END BLOCKS

The presented integration demonstrator contains two bandpass filters, an LNA and a downconversion mixer. The prototype module is intended to demonstrate the concept of SoP. A lot of optimization work on the different blocks, especially on the LNA, is still possible.

An on-package integrated multilayer filter offers a more attractive implementation than on-chip and discrete filters [3]. There is possibility to improve the filter design by making multilayer inductors by having the freedom of equal thickness of metal layers. The size of the inductors influences much on the quality factor. The quality factor improves by increasing the conductor coil width, inner diameter. However, increase in inductance occurs by increasing the number of turns but at the same time if the inductor is drawn on one layer, this causes the decrease in quality factor which in turn increases the insertion loss of the filters. This problem can be solved by designing multilayer inductors explained. All components are matched for 50Ω , which is not necessarily an optimum, but is often a requirement when using of-the-shelf components or when measurement of the separate functions is mandatory.

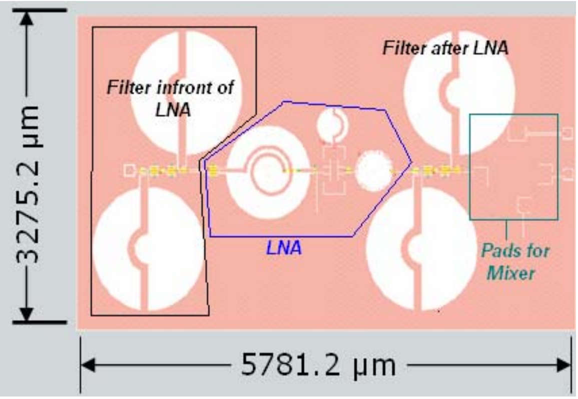

Figure 10: Receiver front-end layout

It consists of a single class A stage. The transistor is available as bare die and is mounted on the MCM-D substrate with the flip-chip technique, explained. All the passives are integrated in the MCM. The low noise amplifier is built around a GaAs high electron mobility transistor [8]. Amplifier is designed to be unconditionally stable, which means that the amplifier is stable for every possible source and load impedance.

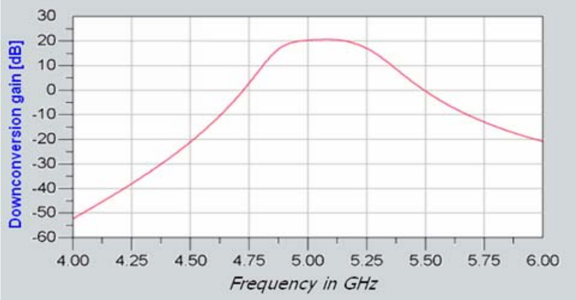

Figure 11. Downconversion Gain

The amplifier consumes 10 mA for a 2 V power supply [8]. Measurements on the LNA separately are shown in section IV.

The downconverter is a GaAs MMIC [9]. The device has a minimum specified gain of 12 dB. The complete receiver front-end layout design is shown in Figure 10 and has a measured conversion gain of 18 dB shown in Figure 11. The whole structure measures 3275 µm by 5781 µm. The conversion gain is with in the acceptable range, it can be further improved by making the filters with more improved performance i.e., with low insertion loss.

VIII CONCLUSIONS

In this document, we have shown the advantages of SoP over single-chip solutions. Single-chip solutions do not provide complete system integration. A SoP approach using an MCM-D technology is a more complete solution that is compact and that is more flexible than a single-chip approach. Moreover, we have demonstrated that high-quality passive components can be embedded on an MCM-D substrate. These passives can be used together with mounted active components as well as for the design of integrated RF bandpass filters and matching networks. We have built prototype SoP-integrated RF modules of a receiver front-end with commercial bare-die components to demonstrate this concept. This receiver has a measured gain of 18 dB, making it suitable to serve as a part of a 5 GHz Wireless LAN system. A single-package approach is neither limited to one certain technology, nor to the availability or limits of commercial components, thus creating more degrees of freedom for design. Also the antenna is a candidate for future integration in the MCM-D module. It has been shown that this is possible.

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