Design and Comparison of Various Passive Components of a 5GHz Wireless LAN Applications

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Abstract: *Future high-performance wireless communication applications such as wireless local area networks (WLANs) around 5 GHz require low power and high quality integrated transceiver solutions. The integration of RF front end especially poses a great challenge to these applications as traditional system on chip (SOC) approach is quite inefficient. A system on package approach can address the problems in an optimum way. In this paper we present a comparison of different passive element fabrication choices. These passives are to be fabricated between different modules on an MCM-D substrate. Inductors and capacitors are compared on the bases of their Q-factors and SRF(self resonance frequency). RF receiver module is implemented using benzocyclobutene (BCB) as interlayer material.*

Keywords: *Integrated passives, integrated RF front ends, multichip module (MCM), system-on-a-chip (Soc), system-on-a-package (SoP), wireless local area network (WLAN), Bezocyclobutene (BCB).*

1. INTRODUCTION

For future wireless communication systems we see an important trend toward more flexible and wideband (multimedia) applications and toward higher carrier frequencies. Good examples of these trends are the upcoming standards for wideband wireless local area networks (WLANs) in the 5-6 GHz band. It is quite a challenging task to design their analog front ends. Apart from high operating frequency critical aspects are the wide band width, large dynamic range and a good linearity.

For portable and battery powered applications, a low power consumption as well as a high level of integration to reduce size and weight are essential. In current digital communication transceivers, the large number of discrete passive components-mainly in the radio front end-is an important bottleneck for further integration. The new implementation paradigm called “system-on-a-package” (SoP)can increase the level of integration of these future wireless trancievers and at the same time reduce power consumption.

In Section 2, we discuss the prospects and limitations of a single-chip approach. In the Section 3, we present the single package approache, which uses a thin film MCM interconnection technology (MCM-D) to interconnect the different system subcomponents. A large number of components(passive) can be integrated using this approach that are required in traditional radios onto the MCM substrate. Starting from a printed wireboard(PWB) radio design, a more compact MCM module could be derived by mounting different active components as bare die or even as packaged components on the MCM substrate by means of flip-chip interconnection technology and by replacing discrete components by passives that are directly integrated into the thin-film multilayer structure.

2. SYSTEM-ON-A-CHIP (SOC) INTEGRATION OF RF TRANSCIEVERS: FEASIBLE OR NOT?

Traditionally, radio front ends have been based on the super-heterodyne architecture that makes use of one or more IFs with image-reject filters on every IF. At the lowest IF frequency, typically an analog bandpass filter with high quality factor (Q) is required for channel selection. The superheterodyne transceiver has a good performance but it is not suited for a high level of integration, mainly because of the different high-Q analog bandpass filters, which are typically implemented as discrete LC, ceramic or surface acoustic wave (SAW) filters .

On the other hand, a high degree of integration is helpful to obtain high performance systems with small sizes and weight, in conjunction with a low power consumption. At first sight it seems that a single chip solution is the best option that even combines the RF front end with the digital signal processing (DSP) core of the transceiver. In this case the most economical technology will be the digital CMOS. During past years much research has been focused on this single-chip CMOS route for RF transceivers [1]-[8], and this has given several trends leading to more integrated transceivers.

2.1 Trends and Problems

Evolution of CMOS technologies allowing Si RF Design—In the majority of today’s front-end implementations, most active components are realized in GaAs (e.g., low-noise amplifiers (LNA), power amplifiers (PA), mixers, antenna switches, etc.) and very often as individually packaged components. In commercial products, the use of CMOS technology is limited to the IF and baseband sections.

In recent years, much research has been devoted toward CMOS integration of RF circuits[1]-[8]. But there are still several problems that could prevent single-chip integration of complete RF front ends in CMOS in the future.

A number of front-end blocks are (and will most likely remain) impossible to integrate in CMOS, e.g., high-Q, RF and IF bandpass filters or antenna swithes.

For some blocks, there is an important performance penalty associated with standard digital CMOS compared to a GaAs or Si (SiGe) bipolar implementation. Depending on the application specific requirements, some of these blocks will have to be kept off-chip and implemented in GaAs, such as very low-noise amplifiers [with noise figure (NF) around 1 dB] and power amplifier with an output power of several watts. Sometimes [7], [9] a power preamplifier is integrated on-chip, but the actual PA is off-chip. Another problem that may prevent the integration of PA is the interference of very large signal at the output of PA with that of the weak one in the receiver front end.

The maximum allowable supply voltage decreases with CMOS technology scaling. As a result the analog front-end blocks realized in deep submicrometer digital CMOS technologies have a smaller headroom. This limits the dynamic range, which may not be allowable in future digital applications.

Mixed-signal Integration— The rationale behind the research in CMOS RF design is the perspective of future single-chip integration of the RF front-end with the digital basband processing circuits in deep submicrometer (standard digital) CMOS technologies. It would be fruitful to present some problems that could prevent single-chip integration of mixed analog-digital tranceivers.

In the single-chip solutions of mixed-signal front ends, the signal-to-noise ratio (SNR) of the analog block can degrade due to coupling between different functional blocks, especially the coupling via the substrate and the power lines from the digital part to the analog blocks. This problem becomes even worse in deep submicrometer technologies with supply voltage scaling, since this will reduce the dynamic range even further. Analog circuits and especially RF circuits typically have a lower yield than digital circuits due to inevitable parametric variations. Single-chip integration in standard CMOS will therefore reduce the yield of the overall system.

On-chip Inductors— In the past few years [10], [11], there has been a trend in silicon RF design to use on-chip inductors. Integrating inductors would allow to eliminate a large part of discrete passives used in many commercial RF front-end implementations. On-chip inductors too have several disadvantages and problems.

The quality factor (Q) of on-chip inductors is very low compared to discrete inductors. Unloaded Qs of on-chip inductors are typically not higher than five. By using several metal layers in parallel or by using thick metal layers, Qs of around ten will probably be feasible in the frequency range 5-6 GHz. By using even more advanced and costly technological solutions (low-*k* dielectrics, Cu metallization), Qs of about 20 are predicted in future deep submicrometer CMOS processes, but this seems to be an upper limit in the frequency range of interest for standard CMOS technologies [11]. High Qs are important in a number of RF blocks, because they are directly related to block performance and power consumption. For example, phase noise of a VCO is inversely proportional to the square of the Q of the LC tank [12] and directly proportional to the amplifier noise figure. The Q of the tank is limited by the component with the lowest Q, which is more often the inductor. Given that increasing the operating power can often reduce noise figure, we can say that power and inductor Q can be traded to achieve a given phase noise specification. High Qs are, e.g., also important to obtain low noise figure in an LNA [11].

The area of inductor and of passive components in general in RF circuits is very large. For example, in the 2.4 GHz WLAN front end described in [13], the passive components (mainly inductors) consume about 60% of the chip area. Since the cost per square millimeter of deep submicrometer silicon processes is increasing rapidly with technology scaling and the size of inductors does not scale, the cost of these integrated inductors will become more and more important in fully integrated RF front ends.

New Architectures — Alternatives for the superheterodyne front-end architecture have been explored recently, to allow higher levels of front-end integration by eliminating high-Q discrete IF bandpass filters: zero-IF [4], [9], low-IF [7], wideband IF double conversion [6] architectures, etc. These architectures have a number of features in common, e.g., the use of quadrature (up-down) conversion and channel selection filtering at (near) baseband frequencies, which can be integrated in CMOS using analog or even digital signal processing. These new architectures also have some disadvantages and problems compared to the classical superheterodyne architectures.

The SNR performance of these architectures based on quadrature conversion is lower than for the traditional superheterodyne architectures. The mirror signal suppression is limited by the imperfect quadrature generation at RF frequencies and mismatches in the in-phase and quadrature (*I/Q*) signals to about 30-40 dB. However, for most digital telecom applications this limitation does not present a problem, and very often the receiver SNR is limited by other effects, e.g., phase noise, distortion, adjacent-channel interference, etc. At least one discrete RF bandpass filter in the receiver (a blocking filter) as well as in the transmitter (to limit out-of-band spurious emissions) is still required.

2.2 Solutions

Some of the problems stated above can probably be solved (at least partially) by further planned developments in deep submicrometer CMOS technologies or by going to specialized, non standard (expensive) technology options.
Antenna switches can probably be implemented by using silicon-on-insulator (SOI) technologies. Very high performance, high frequency RF blocks could be implemented in silicon by going to SiGe BiCMOS technologies. The voltage scaling problem can be eliminated by using BiCMOS technologies, where the

bipolar devices can typically stand higher supply voltages. Other solutions in CMOS technology are triple-well technology and low V_T devices. The substrate coupling problem between analog and digital circuits could be alleviated by going to triple-well technology, deep trench isolation, SOI, etc., and finally, the use of thicker metal layers, Cu metallization or low-*k* dielectrics can increase the quality factor of on chip inductors.

3. SYSTEM-ON-PACKAGE (SOP) INTEGRATION OF RF FRONT ENDS

An alternative implementation of integrated systems is to partition the RF transceiver in multiple chips and to use a thin film multichip module technology (MCM-D) to interconnect these different chips. At the same time, this MCM technology can be used to integrate a large number of the required passive components with very good quality factors. With this implementation approach, several RF components-each implemented in the most suitable IC technology-can be assembled in a relatively simple and economical way [14], [15].

3.1 MCM Technology

Multichip module technologies may be divided into three major categories depending upon the material or processing method of the multilayer stack:

- MCM-L: organic laminate layers
- MCM-C: ceramic layers, generally co-fired
- MCM-D: deposited thin film layers

MCM-L is considered low cost technology, MCM-C is low to medium cost and MCM-D involves relatively high costs, when compared to MCM-L and MCM-C.

Thin-film MCM-Ds are fabricated by a sequential deposition of conductor, typically Cu or Al, and dielectric layers, typically polyimide or benzocyclobutene (BCB), on a substrate base made of ceramic, silicon, or metal. MCM-D processing most closely parallels the processing techniques used in the semiconductor industry. The thin dielectric layers (120 µm thick) are usually deposited by a conventional spin coating process, yielding a uniform and well controlled thickness. Vias can be formed by laser ablation, reactive ion etching, or wet etching of the dielectric. The thin metal layers are deposited by sputtering (tens of nanometers upto few micrometers thick) and patterned by etching. Further additive processing by electroless plating or electroplating (upto 10 µm thick) may also be done. The curing of the dielectric layers require much lower temperature steps compared with low temperature co-fired ceramic (LTCC). Temperatures are in a range of of 200° C (BCB) to 400°C (polyimide). The widths and spaces of the conductors in MCM-D range from about 100 µm down to a few µm, depending on the metal thickness. The IMEC MCM-D technology [16]-[18] consists of alternating thin layers of photosensitive benzocyclobutene (BCB) dielectric and low-loss copper metallizations deposited on low-loss alumina or borosilicate glass carrier substrates. The BCB dielectric has low dielectric losses ($\tan\delta \approx 8.10^{-4}$) and a low dielectric constant ($\varepsilon_r = 2.65$). The material is spin coated in thin films of 1-10 µm thick, then developed and cured. The curing temperature profile of BCB does not exceed 250° C, which is significantly lower than for most other dielectric materials (such as, e.g., polyimide). Depending on the required metal thickness, the metal layers are sputtered and patterned using wet etching or electroplated on a thin titanium-copper seed layer. Via holes through the BCB dielectric allow the connection of the different metal layers. Due to the photosensitive property of BCB, the vias are immediately formed after the developing step. The via diameter is typically 30 µm.

The MCM layer structure can also be used to integrate passives. The TaN resistors (with R =25Ω) and Ta_2O_5 capacitors ($\varepsilon_r = 25$) are realized immediately on the carrier substrate. They are contacted with an aluminum metallization, while the further interconnections and spiral inductors are made using the other high-conductivity copper layers. The top copper layer is coated with NiAu in order to allow easy mounting of other devices (flip-chip (to be discusses later) , wirebonding). The uncovered BCB at the air interface serves also as a passivation layer since it is very stable, very corrosion hard and it has a very low moisture absorption.

3.2 Integrated Passives

Integrated passives are passive electronic components that are fully integrated in a layered carrier structure during fabrication of that structure. This is opposite to discrete passive devices which are passive electronic components surface mounted after fabrication of the carrying structure.

Passives can be integrated using each of the three MCM technologies: MCM-L [16], MCM-C [17]-[23] or MCM-D [24]-[28]. The quality of MCM-L integrated passives is relatively poor and limited to low frequencies. Recently, MCM-L structures with extra thin film layers deposited on top have been presented. In this way, the PWB quality is updated a little (realizing a so called MCM-D/L structure) at the expense of extra cost. In these thin films passives may be integrated. These solutions are unfortunately valid at lower frequencies which obviously is not the case we are pursuing here. At higher frequency the underlying PWB materials will induce high dielectric losses.

The differences between MCM-C and MCM-D with respect to processing technology and use of materials also have an impact on the characteristic of the integrated passives. MCM-D materials have better electrical material properties compared to MCM-C (e.g., tanδ is at least one order of magnitude better). This is especially important when going to higher frequencies. The spin coated thin dielectric layers in MCM-D generally have a much lower dielectric constant compared to ceramic materials. At high frequencies, this translates to longer physical lengths to given electrical lengths which results in easier control of dimension.

The control of the layer thickness and feature dimensions is much better in MCM-D. MCM-C suffers from dimension uncertainties as a result of shrinkage during sintering. The design of embedded passives in MCM-C can become extremely difficult, since true three dimensional design is required. Over 1-2 GHz it poses a great design challenge.

Minimum line widths and spaces in MCM-D are in the order of a few micrometers. In case of LTCC (MCM-C), the required screen printing techniques limit line width and spaces to 100 µm. Recent developments have demonstrated that combinations of LTCC together with photosensitive materials and photodefinition techniques allow the realization of conductor lines and spaces down to 50 µm [20]. This however increases the cost, which reduces the important initial advantage of LTCC.
Moreover, incompatibility problems may occur between different LTCC materials resulting in thermomechanical reliability problems [18]. All these effects have their influence on the quality of passives. With low frequency MCM-C may be used. Also for high power but low frequency applications LTCC may be preferred. Otherwise, MCM-D is required. MCM-D passives have been demonstrated in the range of several tens of GHz. The discussion here is limited to thin film MCM-D case.
Here it would be fruitful to take a look at the advantages that are offered by integrated passives over those of surface mounted devices:

- Improved package efficiency
- Improved electrical and high frequency performance due to reduced parasitics
- Elimination of a separate pacjkage for passive yielding lower cost, and reduced profile weight
- No assembly to board
- Improved reliability due to solder joint failures.

In MCM-D, inductors with values between 1-40 nH with unloaded Qs up to 80 (depending upon inductance value) can be realized, as well as capacitors upto 1 nF/mm^2 (Ta_2O_5).

Capacitors: In MCM-D, capacitors may be realized in different ways [25]. A fisrt type is the classical parallel plate capacitor consisting of a metal-insulator-metal (MIM) build up. The insulating dielectric may be BCB (this case) for small capacitors or anodized tantalum for large values.

A second type consists of two capacitors in series connected through a common floating metal patch. For small capacitance values, this capacitor has the advantage that its size doubles, moving the feature size away from process tolerance prone dimensions. Furthermore the parasitic effects may be reduced using this type of capacitor.

A last type is the radial stub capacitor. This component is narrow at one end and fans out radially on the other. It is generally used as a precise located shunt capacitor to the surrounding ground plane.

Inductors: High quality integrated spiral inductors are hard to realize. In standard silicon the low resistivity of the silicon causes dielectric losses, which limits the quality of the inductor to about five at 1 or 2 GHz. The developments in silicon processing use copper-damascene techniques on low loss substrates to realize higher quality factors upto 15 at 3 GHz for 1.5 nH coils [11]. However these new techniques are quite expensive and not always compatible with the rest of the silicon processing. When realizing the same spiral inductors in MCM-D on a low loss alumina or glass carrier substrate, its quality factor increases tremendously at an overall low cost [24], [25]. Values up to 80 may be achieved at GHz frequencies. The spiral made is multiturn circular and in a coplanar fashion. The center of the spiral is connected to the outside through an overpass using a higher metal layer.

Flip-chip Technology: When flip chip technology is used for mounting different devices on the MCM substrate the advantages are even more obvious since flip-chip interconnections have much smaller parasitics than bonding wires. Several methods such as thermocompression, thermosonic bonding, soldiering and adhesive joining etc, are possible for flip-chip joining [29].

Depending on the bump and the substrate materials, the flip-chip joining can be done in a number of ways. The most well known is soldering, using high or low melting point bumps. For low melting point bumps, the joining process is quite straight forward. The chip is placed in flux or solder paste on the substrate and the assembly is reflowed. The joint is formed through the melting of the actual bump and the paste where applicable. The high melting point bumps, also known as solid core bumps, are joined to the substrate by melting either solder paste or a low melting alloy on the bumps or on the conductors on the substrate. The chip to substrate standoff is well defined and will be greater than or equal to the nonmelting bump height.

Soldering has the significant advantage of self alignment. When soldering flip-chips, the surface tension of the molten solder will pull the chip to its correct position. This means that the mounting does not have to be extremely precise. Limitations of using solder techniques are the realative pitch size (minimum around 500 µm).

Besides soldering, flip chip joins may be formed by thermocompression, where gold bumps and conductors are pressed together during heat exposure. A rule says that when the temperature reaches 300^{o}C, an Au bond can be formed without using ultrasonic energy. Gold wire studs for thermocompression may be placed at very tight pitches (down to 150 µm) with conventional wirebond equipment. This method is very convenient for flip-chip joining of RF chips, since these have low I/O count and benefit from the small dimensions and related minimal parasitics of the studs.

Thermosonic flip-chip bonding is similar to thermocompression except that the temperature and pressure are lowered. The additional energy required to form bonds is provided by ultrasonic means. The impact of ultrasonic energy on the chip has to be investigated to assure that adverse effects remain under control.

Finally, various nonmelting silver bumps using tin solder or adhesives are starting to being used for specific applications. The use of such adhesives is increasing after the European Directive banning of lead in microelectronics from 2004. Accurate modeling of the assembly is necessary to enable design of circuits for loss of the bandpass filter.

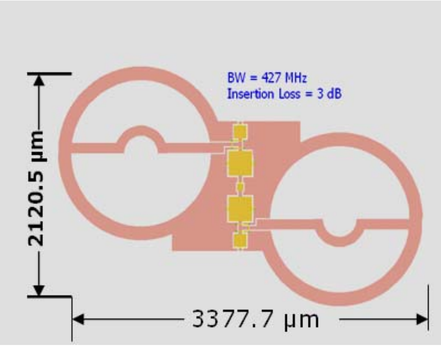

Figure 1. Micrograph of a second order 5-GHz band pass filter

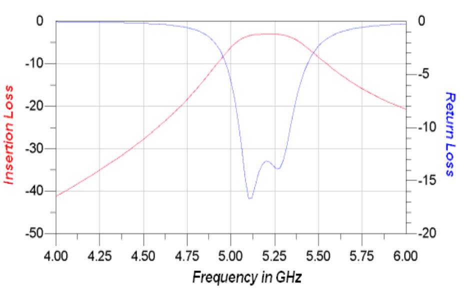

Figure 2. Measured insertion and return

GHz applications. For high frequency design the flip-chip model must include the effect of electromagnetic coupling between the chip and the substrate [30].

4. 5-GHz WLAN RF RECEIVER MODULE

The RF part of a 5-GHz WLAN receiver was implemented using commercial bare die integrated with MCM-D technology. The receiver incorporates two 5-GHz bandpass filters, a low noise amplifier (LNA) and a down –conversion mixer. The 5-GHz RF input frequency is downconverted to an IF of 500 MHz.

The two identical second-order bandpass filters are directly embedded in the MCM substrate. A detailed micrograph is shown in Fgure.1. The measured transfer function of the bandpass filters is shown in Figure.2. The filters show a measured insertion loss of 3 dB and a -1 dB bandwidth of 427 MHz centred around 5.2 GHz. The bandwidth still is with in acceptable limits. The return loss of the filter is around 17 dB. Their size is 3.37 mm by 2.12 mm.

The LNA is built around a GaAs HEMT transistor. This transistor is available as bare die and was mounted with flip-chip technology. The highly linear amplifier is matched for 50 Ω at the output and for the optimal noise at the input. It consists of a single class A stage and has a measured gain of 12.8 dB and a noise figure of 1.42 dB. The size of LNA is 2.5 mm by 1.6 mm. Measured S22 and S11 parameters are given in Figure.3.

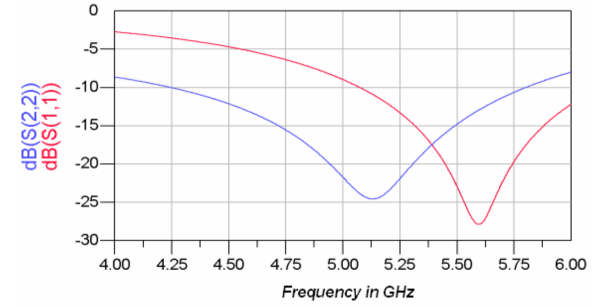

Figure 3. Measured S22 and S11 parameters of LNA.

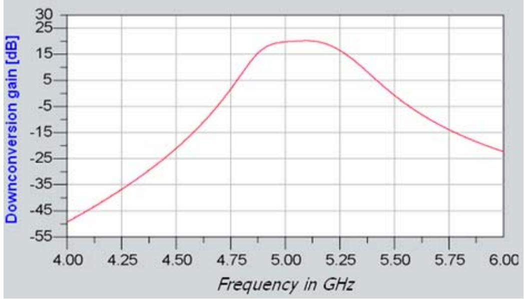

Figure 4. Measurement results of the down-conversion gain of the 5-GHz receiver RF module, consistin

The down-converter is a GaAs MMIC (TGC1411 from Triquint Semiconductor). This device has a minimal gain of 12 dB and consumes 75 mW.

The complete receiver has a measured conversion gain of 17 dB and a noise figure of 9dB. The measured size is 3.5 mm by 6.5 mm. The down-conversion gain of the complete front-end module is shown in Figure.4.

5. CONCLUSION

We have shown that fully integrated single-chip transceivers in standard digital CMOS will probably not be feasible in future, especially for high performance and high-frequency applications such as the new 5-GHz WLAN standards. As an alternative implementation methodology, a system-in-a-package (SoP) approach has been proposed for wireless transceivers. Such a package contains different ASICs that are interconnected with an MCM-D technology. In this technology, high-quality passive components and MEMS can be directly integrated. The SoP implementation approach has been demonstrated with the design of a 5-GHz WLAN receiver front-end module. The high quality factors of the integrated passive components can yield low-power solutions. In some RF circuits (e.g., LNA), the use of higher quality passives means that power consumption can be reduced for the same performance. High quality passives also lead to lower insertion loss for the integrated MCM filters. Less insertion loss in the antenna filter of a transmitter can also lead to a significant power reduction in the power amplifier. Power can also be reduced at the system level using this SoP approach.

The "single package" integrated system design, proposed here as an alternative for single-chip integration, is not incompatible with the expected future improvement of CMOS. It is not a temporary solution that will become obsolete with predicted CMOS technology scaling. Instead, these single package transceivers will only benefit from the evolution in RF CMOS design and the development of new front–end architectures: the resulting single-package solutions will only become denser and cheaper. There will be fewer devices mounted on the MCM substrate, but the cost and performance gain by implementing the large passives in the MCM substrate instead of on-chip will remain. Moreover, a number of RF components will not be integrated on-chip, e.g., RF filters, Tx/Rx switch, antenaas, etc., and these components can be integrated in the package.

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